DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LAB MANUAL

FOR

ELECTRONIC DEVICES & CIRCUITS LAB

Lab Manual Designed By

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MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)
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IMPORTANCE OF EDC LAB

"A practical approach is probably the best approach to mastering a subject and gaining a clear insight."

Electronic Devices and Circuits lab covers those practical oriented Electronic circuits that are very essential for the students to solidify their theoretical concepts. This provides a communication bridge between the theory and practical world of the electronic circuits. The knowledge of these practical are very essential for the engineering students. All of these practical are arranged on the modern electronic trainer boards.

The lab section consists of Diode circuits. Some of the very useful diode based circuits. Labs concerning over this part provides the elementary knowledge of the subject. It also provides some sort of introduction to the lab equipments. This lab also describes the Bipolar Junction Transistor based circuits. Different configurations of BJT amplifier are discussed in this part of the book .Each and every practical provides a great in depth practical concepts of BJT. It also covers some other useful features such as biasing concepts, different type of biasing technique and load line concept, Oscillators and Feedback amplifiers etc. And this lab consists of Field Effect Transistor (FET); one of the leading technologies in electronics is discussed. It gives the introduction to the FET based electronic circuits.

LIST OF EXPERIMENTS

PART A: (Only for Viva-voce Examination)

ELECTRONIC WORKSHOP PRACTICE (in 3 Lab sessions):

1. Identification, Specifications, Testing of R, L, C Components (Colour Codes), Potentiometers, Switches (SPDT, DPDT and DIP), Coils, Gang Condensers, Relays, Bread Boards, PCB‘s.

2. Identification, Specifications and Testing of Active Devices, Diodes, BJT‘s, Low Power JFET‘s, MOSFET‘s, Power Transistors, LED‘s, LCD‘s, SCR, UJT.

3. Study and operation of

- Multimeters (Analog and Digital)
- Function Generator
- Regulated Power Supplies
- CRO

PART B: (For Laboratory Examination – Minimum of 10 Experiments)

1. Forward and Reverse Bias Characteristics of PN Junction Diode.

2. Zener Diode Characteristics and Zener as Voltage Regulator.

3. Input and Output Characteristics of Transistor in CB Configuration.

4. Input and Output Characteristics of Transistor in CE Configuration.

5. Half Wave Rectifiers with & without Filters.

6. Full Wave Rectifiers with & without Filters.

7. FET Characteristics.

8. Measurement of h parameters of transistor in CB, CE, CC Configurations.

9. Frequency Response of CC Amplifier.

10. Frequency Response of CE Amplifier.

11. Frequency Response of Common Source FET Amplifier.

12. SCR Characteristics.

13. UJT Characteristics.

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1. PN JUNCTION DIODE CHARACTERISTICS

AIM:- 1. To Plot the Volt _Ampere Characteristics of PN Junction diode under Forward and Reverse bias Conditions.

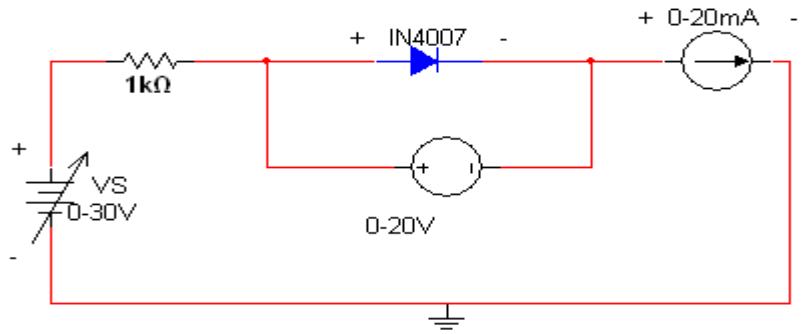
2. To find the static and dynamic forward bias resistance and reverse bias resistance.

APPARATUS REQUIRED:-

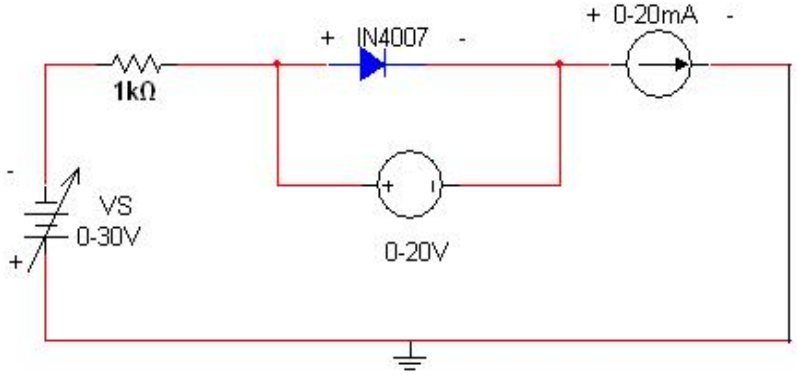
1. IN 4007 Diode(Silicon)	1.No.
2. OA79(Ge)	1.No.
3. Resistor 1KΩ	1.No.
4. 0-20mA DC Ammeter	1No.
5. 0-200 μA DC Ammeter	1.No.
6. 0-20V DC Voltmeter.	1.No.
7. 0-30V Regulated Power Supply	1.No.
8. Bread Board	1.No
9. Connecting wires	set

CIRCUIT DIAGRAMS:-

FORWARD BIAS



REVERSE BIAS



THEORY:

A P-N Junction diode is also called as Semiconductor diode (Ge or Si). When a semi conductor is doped with p type impurity on one half and with N type impurity on the other half and heated to a temperature of 1200^0C then a P-N Junction diode is formed. Junction diode can work in two types of biases.

FORWARD BIAS:

When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage due to majority carriers take part in conduction of current.

REVERSE BIAS:

When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current is due to minority charge carriers.

CUT IN VOLTAGE:

The Forward Voltage at which the current starts to rise abruptly is known as Cut –In voltage of the diode. For Ge is 0.3V, For Si is 0.7V.

PROCEDURE:

FORWARD BIAS CHARACTERISTICS:

1. Make the Circuit connection as per the Circuit Diagram on the bread board
2. The regulated Power supply is switched on and the source voltage is slowly increased and the voltage across the PN Junction diode insteps of 0.1Volt is noted down and the Corresponding diode currents are noted down under forward bias Condition in table given below.
3. The graph V_f versus I_f is plotted on the graph Sheet to the scale.
4. The dynamic forward bias resistance of the diode is calculated from the graph

$$r = \frac{\Delta V}{\Delta I}.$$

5. The cut in Voltage of the diode is observed and noted down.

TABLE:

FORWARD BIAS CHARACTERISTICS:

S.N o	Forward Bias Voltage (Vf) in volts		Forward Bias Current (If) in mA	
	Ge	**Si**	**Ge**	**Si**
1				
2				
3.				
4.				
5.				
6.				
7.				

REVESE BIAS CHARACTERISTICS:

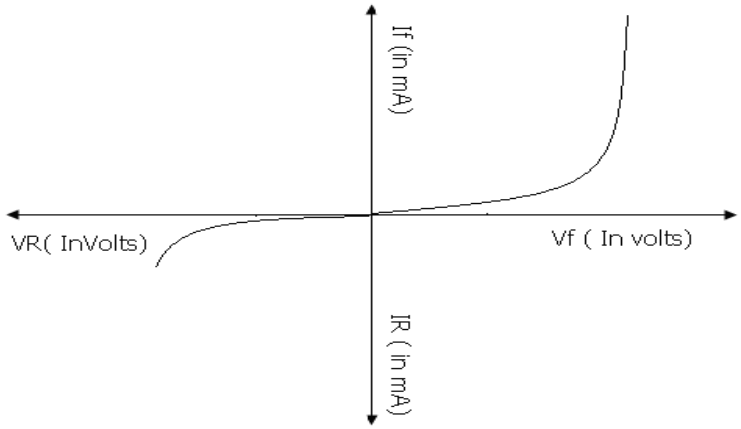
1. The Circuit is connected as per the Circuit Diagram on the bread board.
2. The regulated Power supply is switched on and the source voltage is slowly increased and the voltage across the PN Junction diode insteps of 1Volt is noted down and the Corresponding diode currents are noted down under reverse bias Condition in the table given below.
3. The graph Vr versus Ir is plotted on the graph Sheet to the scale.
4. the dynamic reverse bias resistance of the diode is calculated from the graph.

$$r = \frac{\Delta V}{\Delta I}$$

REVERSE BIAS CHARACTERISTICS:

S.N o	Reverse Bias Voltage (Vr) in Volts		Reverse Bias Current (Ir) in μ A	
	Ge	**Si**	**Ge**	**Si**
1				
2				
3.				
4.				
5.				
6.				
7.				
8.				

MODEL GRAPH:



RESULT :

The V-I Characteristics of the PN Junction diode are plotted for the Both forward and reverse bias conditions and Calculated the dynamic forward and reverse bias resistance.

QUESTIONS:

1. Define forward resistance and Reverse Resistance, What are the approximate values from the graph?
2. Define Cut in voltage of a diode, mention the cut in voltage for Ge & Si?
3. Explain the working of PN Junction in Forward and Reverse Bias conditions?
4. Define depletion region of a diode?
5. What is meant by transition & space charge capacitance of a diode?
6. Is the V-I relationship of a diode Linear or Exponential?
7. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
8. What are the applications of a p-n diode?

2. ZENER DIODE CHARACTERISTICS

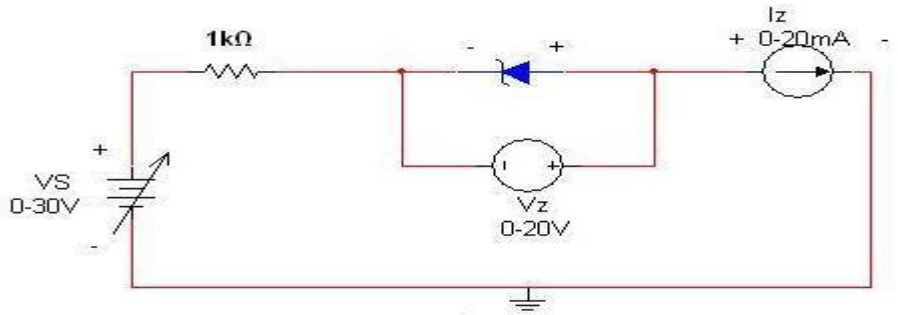
AI M:- To Obtain the Voltage – Current characteristics of a Zener diode and find out the Zener Break down Voltage from the Characteristics.

APPARATUS REQUIRED:-

1. D.C Regulated Power Supply 0-30V 1No.
2. Zener Diodes -3.9V,-8.2V Each 1No.
3. Resistor 1 KΩ & 680 Ω 1No.
4. DC Ammeter 0-20mA 1No.
5. DC Voltmeters 0-1V,0-10V Each 1No.
6. Decade Resistance Box 1No.
7. Bread Board. 1No.

CIRCUIT DIAGRAMS:-

REVERSE BIAS CHARACTERISTICS:-

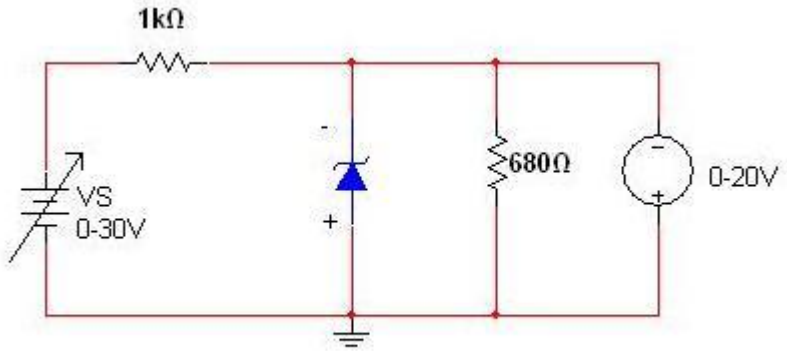


TABULAR FORMS:-

CASE I. REVERSE BIAS CHARACTERISTICS:-

S.No	Source voltage(Vs) in volts	Zener diode voltage (Vz) in volts	Zener diode current (Iz) in mA
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			

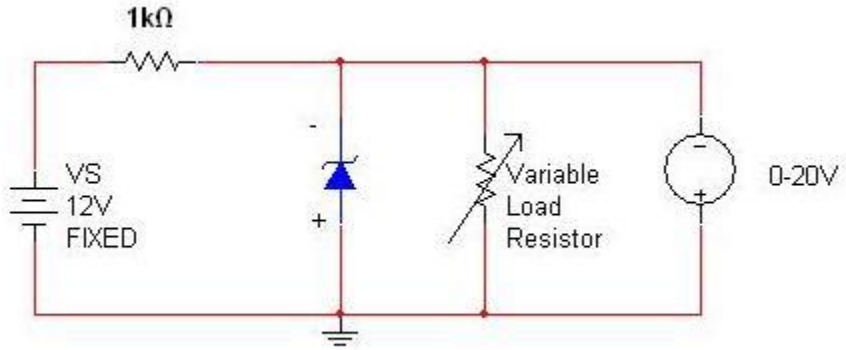
CASE II . REGULATION WITH VARYING INPUT VOLTAGE :



TABULAR COLUMN:

S. No	Source Voltage(Vs) in Volts	Load voltage (V_L) in volts	Load Current (I_L)in mA $I_L = V_L / R_L$
1			
2			
3			
4			
5			
6			
7			
8			

CASE III .REGULATION WITH VARYING LOAD RESISTANCE :



TABULAR COLUMN:

S.No	Load Resistance (R_L) in KΩ	Load Voltage(V_L) in Volts	Load Current in mA $I_L = V_L / R_L$
1			
2			
3			
4			
5			
6			
7			
8			

THEORY :

CASE(I) :

The Diodes which are designed with adequate power dissipation to operate in the break down region are known as Break Down (or) Zener diodes. These diodes are employed as constant voltage sources.

CASE(II) :

a) As the input voltage increases, the input current also increases. This increase the current through the Zener Diode with out affecting the load current.
b) The increase in the input current will also increases the voltage drop across the series resistance (R_L), there by keeping the load voltage (V_L) as constant.

CASE(III) :

a) When the load resistance decreases the load current increases.
b) This causes the Zener current to decrease. As a result of this the input current and voltage drop across series resistance remains constant. Thus the load voltage is kept constant.

PROCEDURE:-

CASE(I) : Reverse bias characteristics

1. Make the connections as per the circuit diagram.
2. Switch the DC Regulated power supply and slowly increase the source Voltage and note down the Voltage across Zener diode insteps of the 1Volt and note the Corresponding diode current as per table given below.
3. Repeat the above procedure for the 9.1V Zener diode.
4. Plot the graph between Voltage across the Zener diode (Vr) Vs current (Ir) through the diode on graph sheet for the both zener Diodes.

CASE (II): REGULATION WITH VARYING INPUT VOLTAGE

a) M a k e t h e c o n nections as per the circuit diagram.
b) Keep the input voltage from 0 – 10V in steps of 1 V and note down the readings of source voltage(V_s) , Load voltage (V_L) , Load current (I_L) . c) Plot the graph between I_L Versus V_L.

CASE(III) : REGULATION WITH VARYING LOAD RESISTANCE

a) M a k e t h e c o n nections as per the circuit diagram
b) Keep the input voltage constant at 12V and note down the current with out load resistance. Note this as No load voltage.
c) Slowly vary the load resistance in steps of 1KΩ to up to 10KΩ and note down the corresponding meter readings. Calculate the regulation by using the formula.

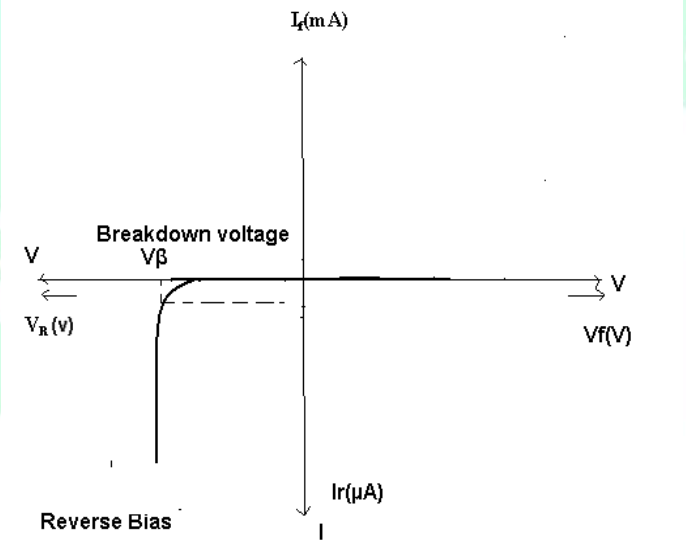
$$(V_{NL} - V_{FL}) / V_{FL}$$

d) Plot the graph between I_L Versus V_L.

ZENER BREAK DOWN VOLTAGE:-

Draw the tangent on the reverse bias Characteristics of the Zener Diode starting from the Knee and touching most of the points of the Curve.
The point where the Tangent intersects the X-axis is the Zener Break down Voltage.

MODEL GRAPH:-



RESULT:- The V- I Characteristics of the Zener Diode and the Zener Break Down Voltage from the Characteristics are Observed.

QUESTIONS:

1. What type of temp? Coefficient does the zener diode have?
2. If the impurity concentration is increased, how the depletion width effected?
3. Does the dynamic impendence of a zener diode vary?
4. Explain briefly about avalanche and zener breakdowns?
5. Draw the zener equivalent circuit?
6. Differentiate between line regulation & load regulation?
7. In which region zener diode can be used as a regulator?
8. How the breakdown voltage of a particular diode can be controlled?
9. What type of temperature coefficient does the Avalanche breakdown has?
10. By what type of charge carriers the current flows in zener and avalanche breakdown diodes?

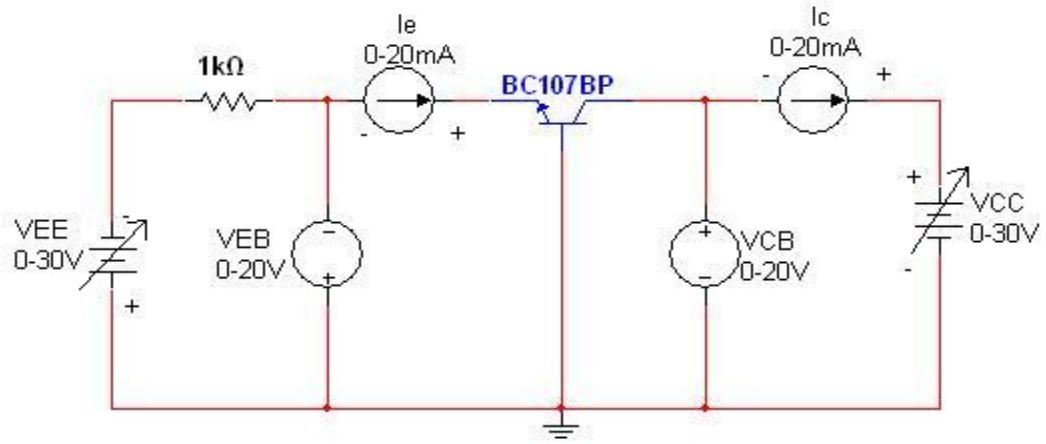
3. TRANSISTOR CHARACTERISTICS IN CB CONFIGURATION (INPUT AND OUTPUT)

AIM: To plot the family of input and output characteristics of a transistor connected in Common Base Configuration.

APPARATUS:

1. Transistor BC 107	1No.
2. Resistor 1KΩ	1No.
3. Ammeter 0-20mA	2No.
4. Voltmeter 0-20V	2No.
5. Multimeter	1No.
6. 0-30V, 1A Dual Channel powers supply	1No.
7. Bread Board	1No.
8. Connecting wires	set

CIRCUIT DIAGRAM:



THEORY :

In the common Base configuration input is applied between emitter and base , similarly output is taken from collector and base. Here base of the transistor is common to both input and output circuits and hence the name common base configuration.

Input characteristics are similar to forward bias characteristics of a P-N junction diode .The curve shift left with increase in VCB value. Output characteristics can be obtained by varying the out put voltage and noting the out put current. The characteristics have been divided in to three regions namely active, saturation and cut off region. But BJT has low input resistance and high output resistance in Common Base configuration.

PROCEDURE:

INPUT CHARACTERISTICS:

1. Make the connections as per the circuit diagram.
2. Make VCB open and vary the Power Supply (Channel-1) and note the Values of

I_E and V_{BE} by increasing the I_E in steps of 0.5mA

3. Adjust V_{CB} = 1V (Channel -2) Power supply.
4. Vary the 0-30V(Channel -1) power Supply and note down the Values of I_E and V_{EB}.
5. Repeat the steps 3 & 4 For V_{CB} = 2V, 3V, 4V.

TABULAR FORM:-

S.No	V_{CB} = 0V		V_{CB} = 3V		V_{CB} = 6V	
	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)
1	0.1		0.1		0.1	
2	0.2		0.2		0.2	
3	0.3		0.3		0.3	
4	0.4		0.4		0.4	
5.	0.5		0.5		0.5	
6.	0.6		0.6		0.6	
7.	0.7		0.7		0.7	
8.	0.8		0.8		0.8	
9.	0.9		0.9		0.9	

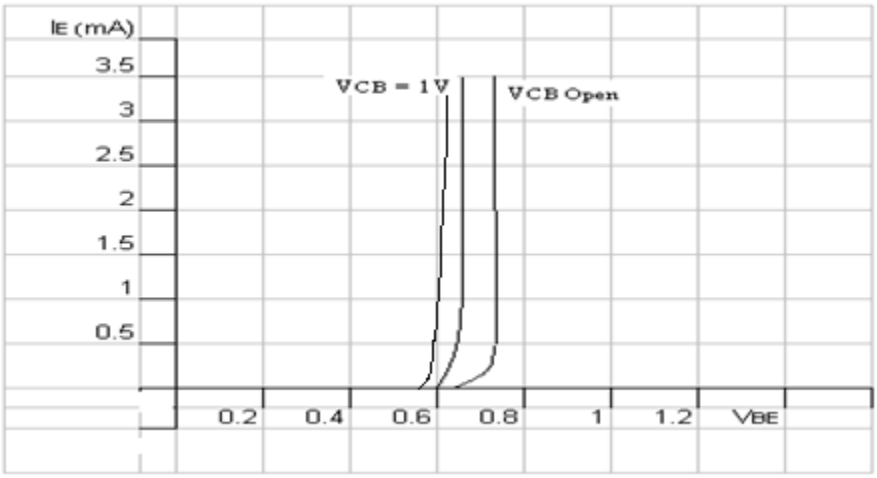
OUTPUT CHARACTERISTICS:-

1. Make the connections as per the circuit diagram
2. Adjust the 0 – 30V (Channel – 1) power supply and fix the value of Ie=2 mA
3. Vary the 0 – 30 V (Channel – 2) power supply and note the value of V_{CB} and I_C.
4. Vary the VCB in steps of 1v
5. Repeat steps 2 to 4 for I_E = 1mA, 1.5mA, 2mA, 2.5mA

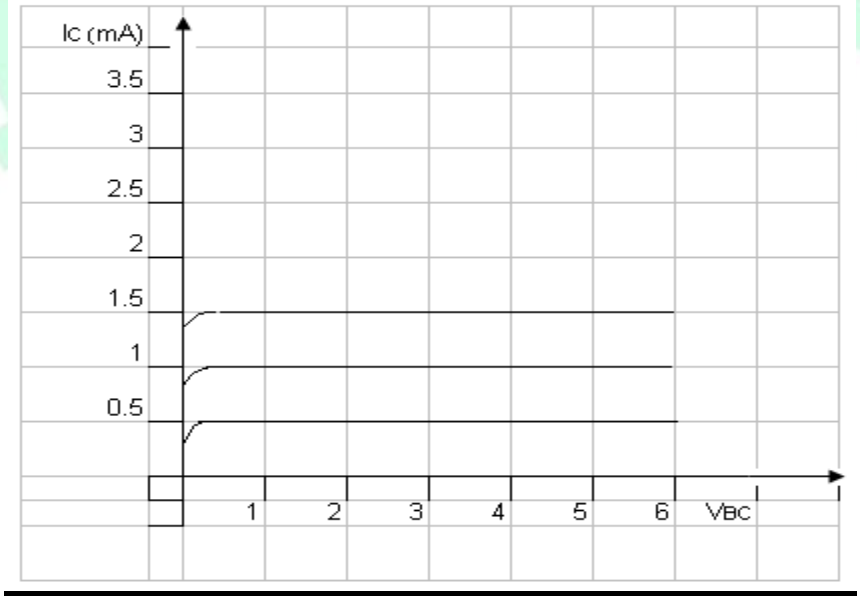
TABULAR FORM:-

S.No	IE= 2mA		IE=4mA		IE=6mA	
	V_{CB}(v)	Ic(mA)	V_{CB}(v)	Ic(mA)	V_{CB}(v)	Ic(mA)
1	1		1		1	
2	2		2		2	
3	3		3		3	
4	4		4		4	
5	5		5		5	
6	6		6		6	
7	7		7		7	
8	8		8		8	

GRAPH:- INPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS :



1. Plot the input characteristics by taking I_E on y – axis and V_{EB} on X – axis
2. Plot the output characteristics by taking Ic on y – axis and V_{CB} on X – axis

RESULT: - Input and Output characteristics are plotted

QUESTIONS:

1. Define transistor and mention types of transistors. Draw their symbolic diagram and indicate terminals?
2. What are the three configurations of Transistor?
3. In which region transistor acts as an Amplifier?
4. In which region transistor acts as an Switch?
5. Why transistor is called current controlled device?
6. What is meant by Base width modulation?
7. What is the range of α for the transistor?
8. Draw the input and output characteristics of the transistor in CB configuration?
9. Identify various regions in output characteristics?
10. What are the applications of CB configuration?
11. What are the input and output impedances of CB configuration?
12. Define α(alpha)? What is the relation between α and β?
13. What is EARLY effect?
14. Draw diagram of CB configuration for PNP transistor?
15. What is the power gain of CB configuration?
16. Which biasing techniques are used for both input and output?

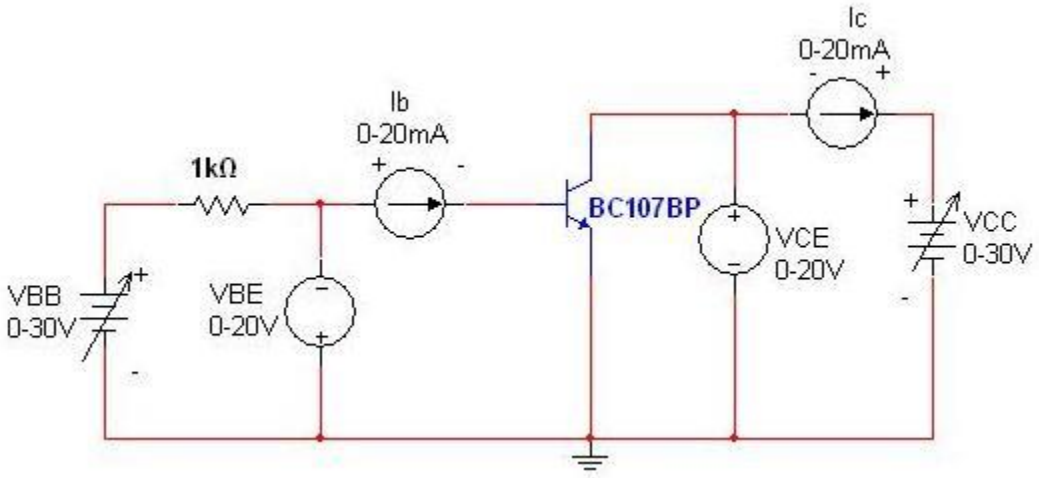
4. TRANSISTOR CHARACTERISTICS IN CE CONFIGURATION (INPUT AND OUTPUT)

AIM: **To** Plot the Family of input and output Characteristics of a Transistor connected in Common Emitter Configuration.

APPARATUS REQUIRED:

1. Transistor BC 107	1No.
2. Resistor 1KΩ	1.No.
3. Connecting Wires	1 Set
4. Ammeter 0-20mA, 0-500 μ A	1 Each
5. Multimeter	1No.
6. 0-30,1A Dual Channel power supply.	1.No.
7. Bread Board	1No.

CIRCUIT DIAGRAM:



THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals . Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE . Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE} at constant I_B. The collector current varies with VCE unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B.

PROCEDURE:

INPUT CHARACTERISTICS

1. Make the connections as per the circuit diagram.
2. Make V_{CE} Open and Vary the 5 V Supply (Channel 1) and note the Values of I_B and V_{CE}, by increasing the I_B in Steps of .5mA.
3. Adjust V_{CE} = 1V in Channel 2 Power supply.
4. Vary the 0-5V (Channel 1) power Supply and note the Values of I_B and V_{BE}
5. Repeat the Steps 3 and 4 for V_{CE} = 2V ,3V,4V.
6. Need not connect 0-2mA(I_C Measurement), Ammeter while taking the input Characteristics.

TABULAR FORM:

S.No	V_{CB} = 0V		V_{CB} = 3V		V_{CB} = 6V	
	VBE(V)	IB(uA)	VBE(V)	IB(uA)	VBE(V)	IB(uA)
1	0.1		0.1		0.1	
2	0.2		0.2		0.2	
3	0.3		0.3		0.3	
4	0.4		0.4		0.4	
5.	0.5		0.5		0.5	
6	0.6		0.6		0.6	
7.	0.7		0.7		0.7	
8	0.8		0.8		0.8	

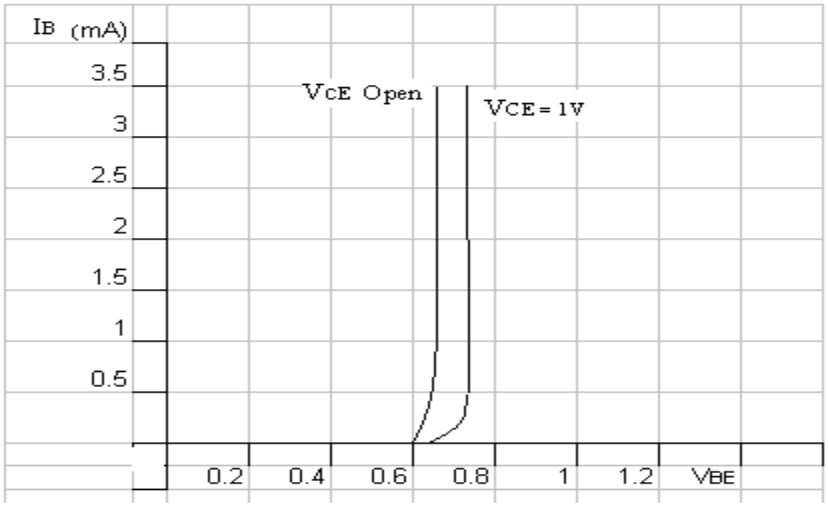
OUTPUT CHARACTERISTICS:

1. Make the connections as per the circuit diagram.
2. Connect 0-500 μ A Ammeter in place of 0-20mA.
3. Adjust 0-5V (Channel -1) power Supply and fix the Values of I_B = 10 μ A
4. Vary the V_{CE} 0-20V (Channel -2) power supply and note down the Values of the Ic and V_{CE}. Vary in the Steps of 1V.
5. Repeat the steps 3 & 4 for I_B = 30 μ A, 40 μ A, 50 μ A .

TABULAR FORM:

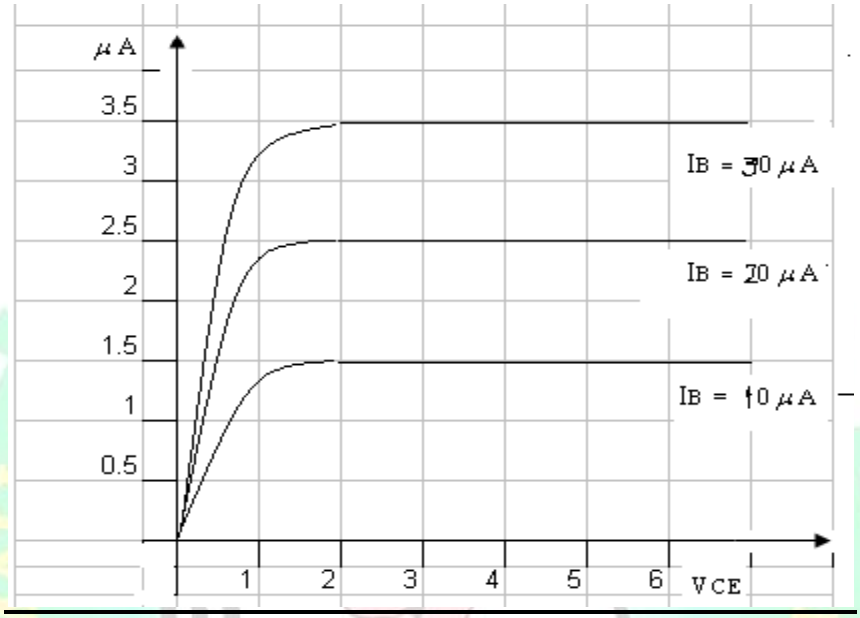
S.No	I_B = 10 uA		I_B = 20 uA		I_B = 30 uA	
	V_{CE}(mA)	I_c(mA)	V_{CE}(mA)	I_c(mA)	V_{CE}(mA)	I_c(mA)
1	1		1		1	
2	2		2		2	
3	3		3		3	
4	4		4		4	
5	5		5		5	
6	6		6		6	
7	7		7		7	
8	8		8		8	
9	9		9		9	
10	10		10		10	

GRAPH: INPUT CHARACTERISTICS



1. Plot the input characteristics by taking IB on Y-Axis and VBE on X-Axis.
2. Plot the output characteristics by taking IC on the Y-Axis and VCE on X –Axis

OUTPUT CHARACTERISTICS:



RESULT:

Input and output characteristics of CE are plotted.

QUESTIONS:

1. What is meant by α *and* β in a CE transistor Characteristics?
2. What are the input and output impedances of CE configuration?
3. Identify various regions in the output characteristics?
4. what is the relation between α *and* β?
5. Define current gain in CE configuration?
6. Why CE configuration is preferred for amplification?
7. What is the phase relation between input and output?
8. Draw diagram of CE configuration for PNP transistor?
9. What is the power gain of CE configuration?
10. What are the applications of CE configuration?

5. RECTIFIER WITHOUT FILTERS (HALFWAVE & FULLWAVE)

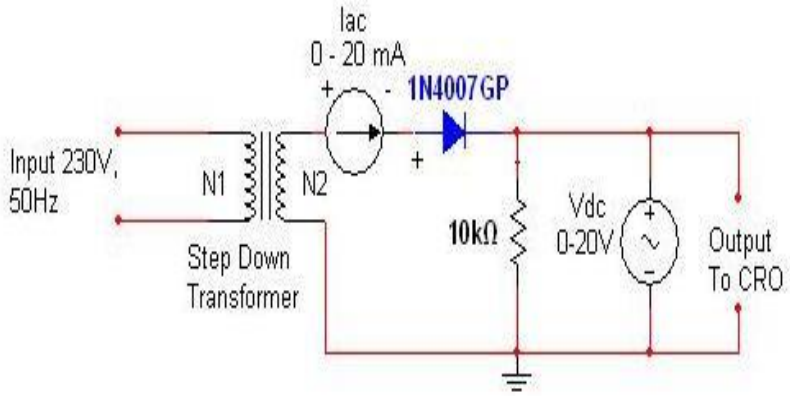
AIM: To rectify the signal and then to find ripple factor, efficiency and percentage of regulation in full wave and half wave rectifier without filters.

APPARATUS:

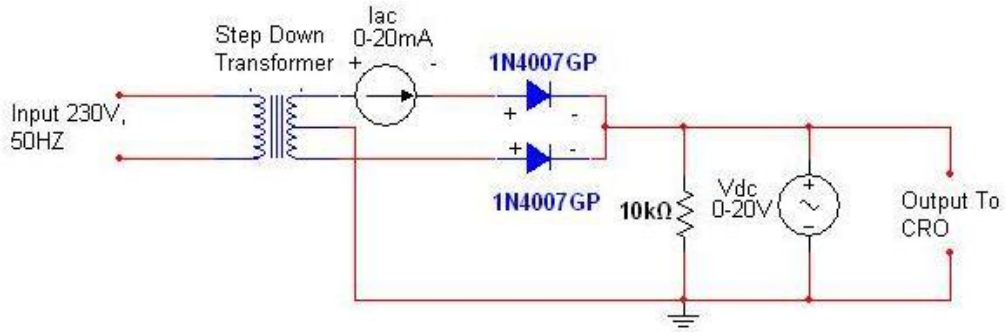
1. Transformer 230v/6v – 0 – 6v
2. Diodes IN4007 2 No
3. R esistance 10k
4. Multimeter
5. Bread Board
6. 20MHz Dual Trace CRO
7. Connecting wires

CIRCUIT DIAGRAM:

HALFWAVE RECTIFIER:



FULLWAVE RECTIFIER:



THEORY:

A Half wave Rectifier is one which converts the ac voltage in to a pulsating dc voltage using only one half cycle of the applied voltage. Rectifier conducts during one half cycle only. During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.

During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

PROCEDURE:

COMMON TO HALFWAVE RECTIFIER &FULLWAVE RECTIFIER:

1. Connecting the circuit on bread board as per the circuit diagram
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the R_L value to 500Ω
4. connect the Multimeter at output terminals and vary the load resistance (DRB) from 500Ω to 5KΩ and note down the Vac and Vdc as per given tabular form.
5. Disconnect load resistance (DRB) and note down No load voltage Vdc.
6. Connect load resistance at 5KΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet

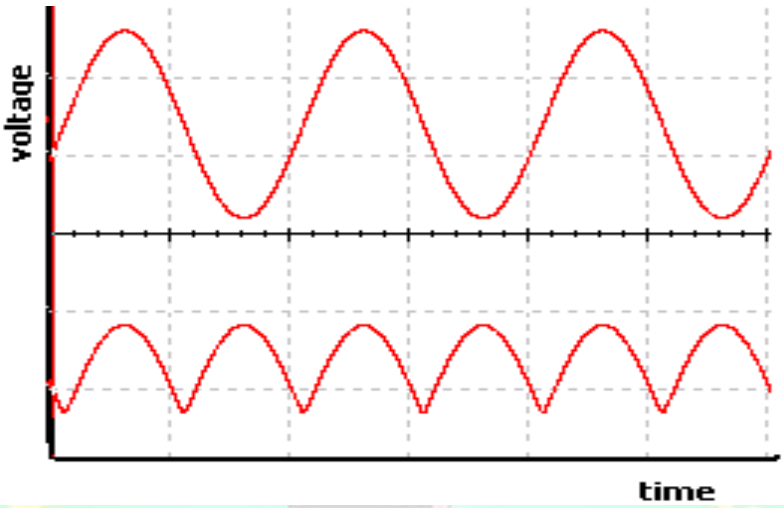
CALCULATIONS:

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 6
2. Calculate Ripple Factor $\gamma = \frac{Vrms}{Vdc}$
3. Calculate Percentage of regulation = $\frac{Vnoload - Vfull\ load}{Vfull\ load} \times 100\%$
4. Calculate efficiency $\eta = P_{dc} / P_{ac}$

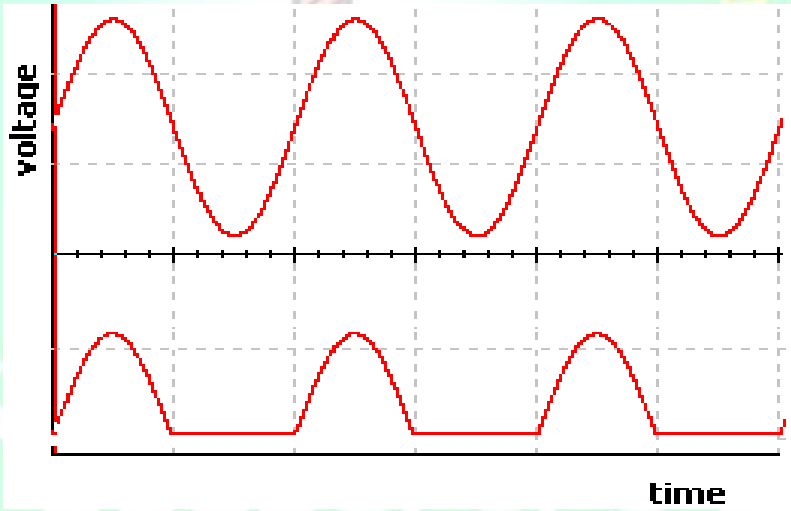
   $P_{dc} = V_{dc} \times I_{dc} = V_{dc}^2 / R_L$

   Pac = Vac x Iac

WAVE SHAPES:



FULL WAVE WITHOUT FILTER



HALF WAVE WITHOUT FILTER

RESULT:

Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Fullwave and Half wave rectifiers without filter.

QUESTIONS:

1. What is the PIV of Half wave rectifier?
2. What is the Ripple factor, efficiency, % of Regulation o f Rectifier?
3. What is the rectifier?
4. What is the difference between the half wave rectifier and full wave Rectifier?
5. What is the o/p frequency of Bridge Rectifier?
6. What are the ripples?
7. What is the function of the filters?
8. What is TUF?
9. What is the average value of o/p voltage for HWR?
10. What is the peak factor?

6. RECTIFIER WITH FILTERS (HALFWAVE & FULLWAVE)

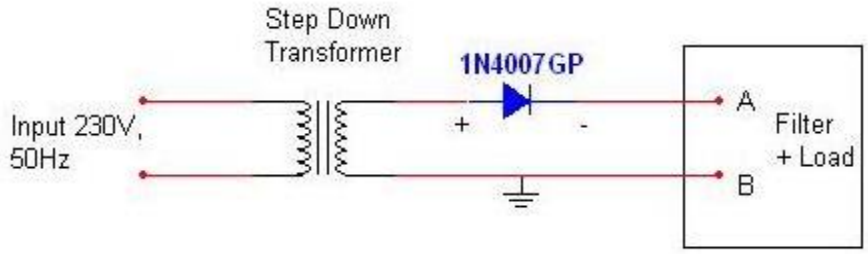
AIM: To rectify the signal and then to find ripple factor in full wave and half wave rectifier with filters.

APPARATUS:

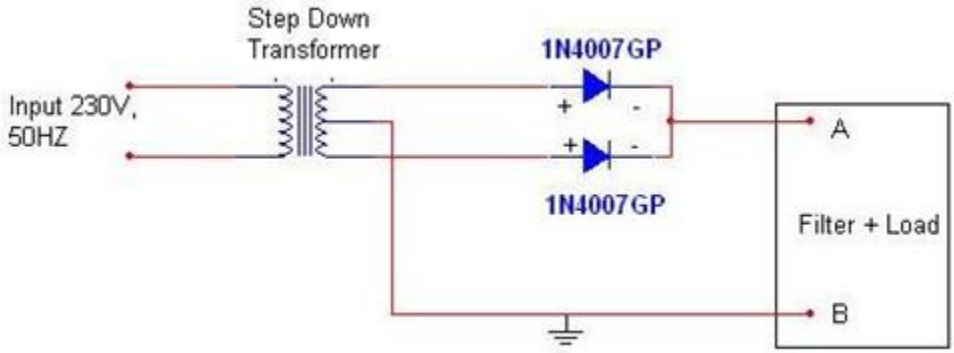
1 .Transformer 230v/6v – 0 – 6v
2. Diodes IN4007 - 2 no's
3 . Capacitor 470µf/35v - 1 no.
4 . Decade Inductance Box
5. Resistance 1K
6. Multi meter
7 . Bread Board
8. 20MHz Dual Trace CRO
9. Connecting wires

CIRCUIT DIAGRAM:

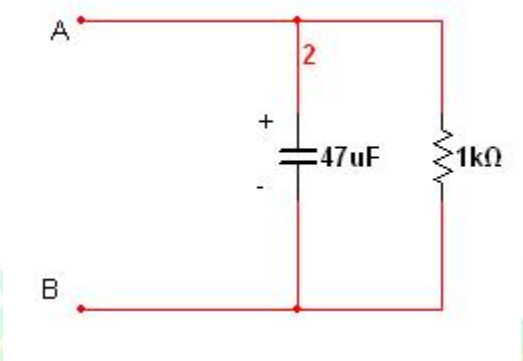
HALFWAVE RECTIFIER:



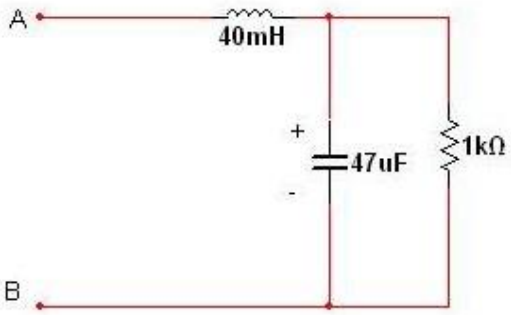
FULLWAVE RECIFIER :



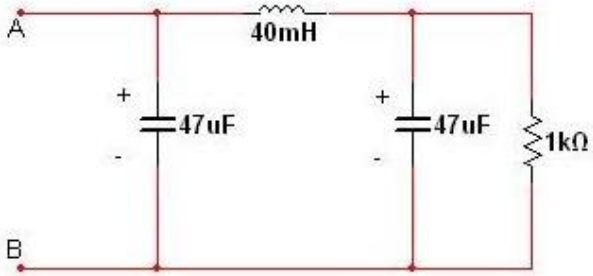
C – FILTER:



L-C FILTER:



CLC – FILTER:



PROCEDURE:

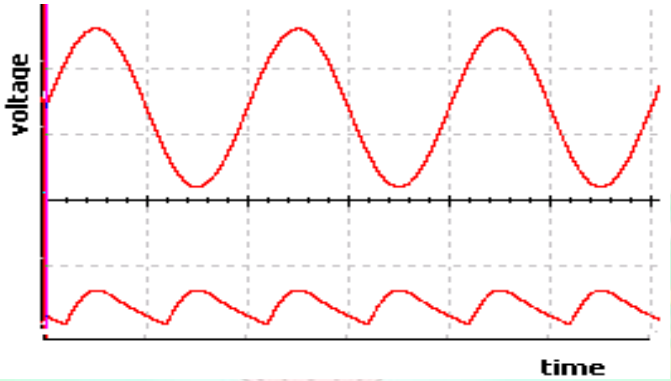
FULLWAVE RECTIFIER:

1. Make the connections as per the circuit diagram
2. Make the connection of primary transformer to main supply i.e. 230V, 50Hz
3. Make the connection of decade resistance box and set the R_L value to 100Ω
4. Make the connection of multimeter at output terminals and vary the load resistance (DRB) from 100Ω to 5KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance (DRB) and note down No load voltage Vdc
6. Make the connection of load resistance at 100KΩ and connect CH – I of Dual Trace CRO at Secondary (Input) terminals, Channel – II of Dual Trace CRO at output terminals and observe and note down the Input and Output Wave form on Graph Sheet

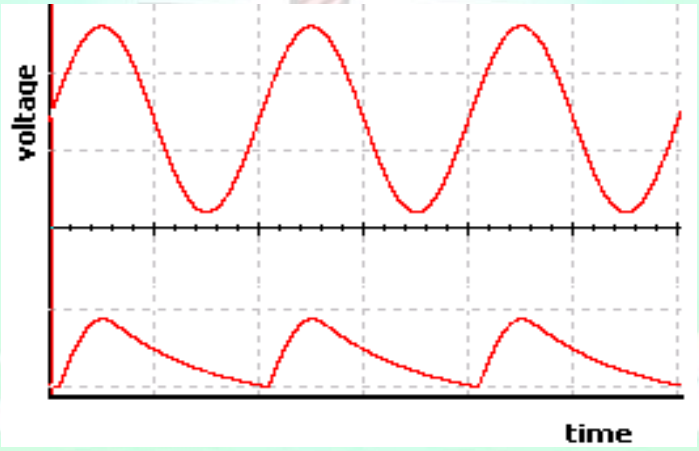
HALFWAVE RECTIFIER:

7. Make the connections as per the circuit diagram and repeat the above procedure from steps 2 to 6 Calculate Ripple Factor $\gamma = V_{rms} / V_{dc}$

WAVE SHAPES:



FULL WAVE WITH FILTER



HALF WAVE WITH FILTER

RESULT: Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full wave and Half wave rectifiers with capacitor filter

QUESTIONS:

1. What is the need of filter?
2. Why we are using L & C components in the filter?
3. What are the types of filters?
4. Which is the best among the different types of filters?

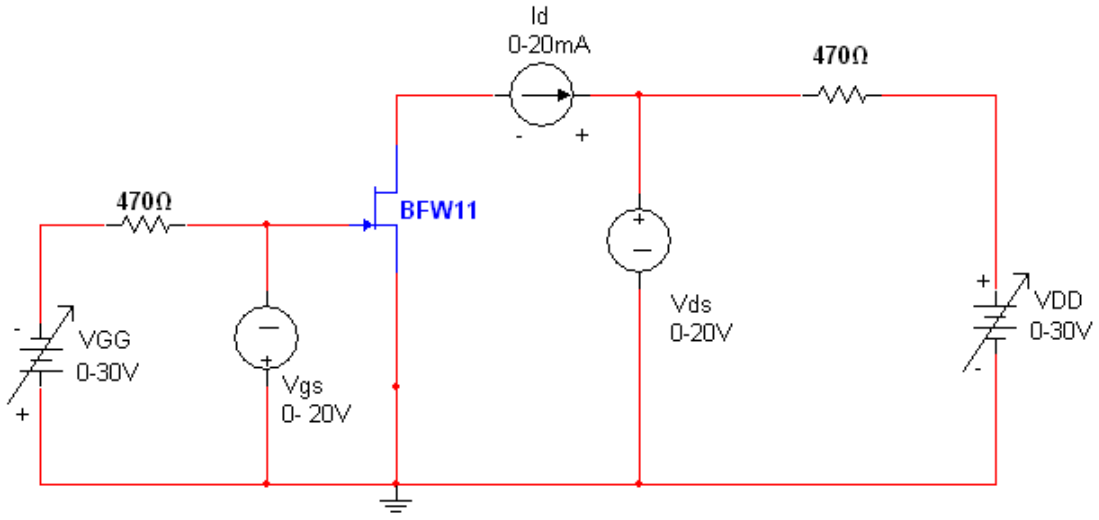
7. FET CHARACTERISTICS

AIM: To plot Output Characteristics and Transfer Characteristics of Field Effect Transistor (FET)

APPARATUS:

1.	FET BFW – 10/11	1 No.
2.	Resisters – 470 Ω	2 No.
3.	Connecting Wires	
4.	Ammeter 0 – 20 Ma	1 No.
5.	Multimeter	1 No.
6.	0 – 30v, 1A Dual Channel Power Supply	1 No.
7.	Bread Board Trainer	1 No.

CIRCUIT DIAGRAM:



THEORY:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with $V_{DS.}$ With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called "pinch of voltage".

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased.

In amplifier application, the FET is always used in the region beyond the pinch-off.

$$I_{DS} = I_{DSS}(1-V_{GS}/V_P)^2$$

PROCEDURE:

TRANSFER CHARACTERISTICS

1. Make the connections as per the circuit diagram
2. Make V_{GS} =1v, by adjusting 0 – 15v (Channel – II) power supply
3. Adjust the 0 – 5v (Channel – I) power supply and note the values of I_D and V_{DS} with the variation of V_{GS} in step of 0.2v, as per table given below
4. Repeat the above procedure for V_{DS}=2v and 3v

DRAIN CHARACTERISTICS

1. Make the connections as per the circuit diagram
2. Make V_{GS} =0v, by adjusting 0 – 5v (Channel – I) power supply
3. Adjust the 0 – 15v (Channel – II) power supply and note the values of I_D and V_{DS} with the variation of V_{DS} in step of 1v, as per table given below
4. Repeat the above procedure for V_{GS}=0.5v and 1v

TABULAR FORM:

DRAIN CHARACTERISTICS:

V_{GS}=0v		V_{GS}= -0.5v		V_{GS}=-1v	
$V_{DS(V)}$	$I_{D(mA)}$	$V_{DS(V)}$	$I_{D(mA)}$	$V_{DS(V)}$	$I_{D(mA)}$
0		0		0	
1		1		1	
2		2		2	
3		3		3	
4		4		4	
5		5		5	
6		6		6	
7		7		7	
8		8		8	
9		9		9	
10		10		10	

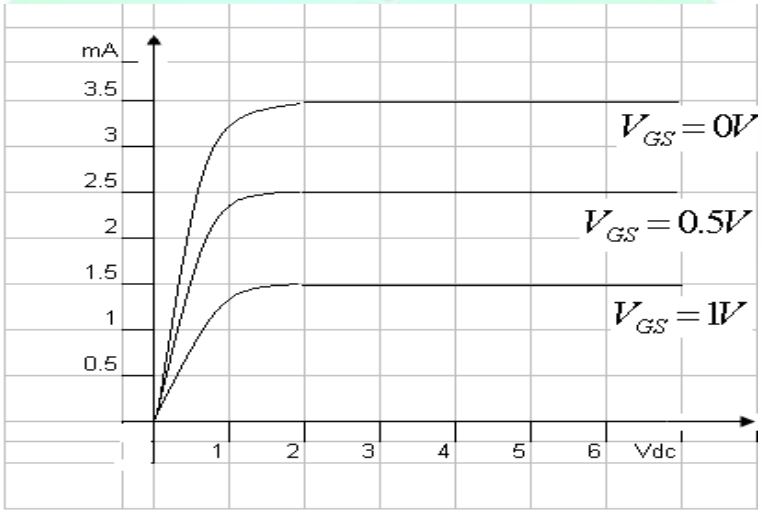
TRANSFER CHARACTERISTICS:

V_{DS}= 1V		V_{DS}= 2V		V_{DS} =3v	
V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)	V_{GS} (V)	I_D(mA)
0		0		0	
0.5		0.5		0.5	
1.0		1.0		1.0	
1.5		1.5		1.5	
2.0		2.0		2.0	
2.5		2.5		2.5	
3.0		3.0		3.0	
3.5		3.5		3.5	
4.0		4.0		4.0	
4.5		4.5		4.5	
5.0		5.0		5.0	
5.5		5.5		5.5	
6.0		6.0		6.0	

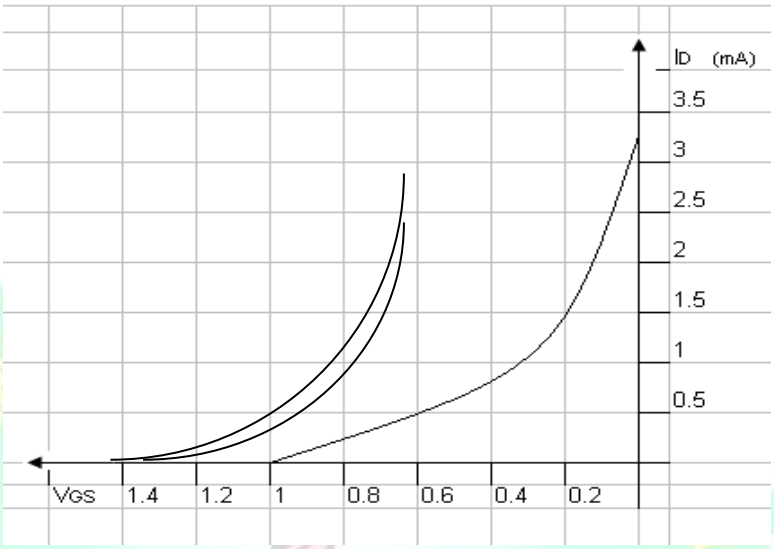
GRAPH:

1. Plot the Output Characteristics by taking I_D on Y-axis and V_{DS} on X-axis for constant values of V_{GS}
2. Plot the Transfer Characteristics by taking I_D on Y-axis and V_{GS} on X-axis for constant values of V_{DS}

DRAIN CHARACTERISTICS:



TRANSFER CHARACTERISTICS:



RESULT:

Output Characteristics and Transfer Characteristics of FET are plotted

QUESTIONS:

1. What are the advantages of FET?
2. Different between FET and BJT?
3. Explain different regions of V-I characteristics of FET?
4. What are the applications of FET?
5. What are the types of FET?
6. Draw the symbol of FET.
7. What are the disadvantages of FET?
8. What are the parameters of FET?

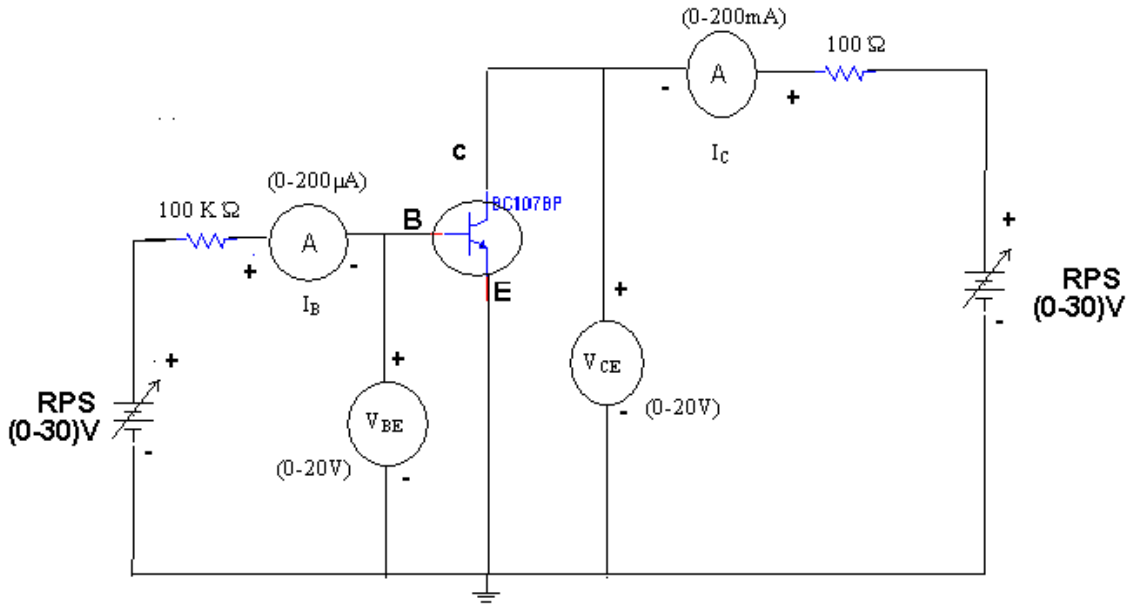
8. MEASUREMENT OF h - PARAMETERS IN CE CONFIGURATION

AIM: To calculate the h-parameters of transistor in CE configuration.

APPRATUS:

Transistor BC 107
Resistors 100 K Ω 100 Ω
Ammeter (0-200μA), (0-200mA)
Voltmeter (0-20V) - 2Nos
Regulated Power Supply (0-30V, 1A) - 2Nos
Breadboard

CIRCUITDIAGRAM:



THEORY:

INPUT CHARACTERISTICS:

The two sets of characteristics are necessary to describe the behavior of the CE configuration one for input or base emitter circuit and other for the output or collector emitter circuit.

In input characteristics the emitter base junction forward biased by a very small voltage V_{BB} where as collector base junction reverse biased by a very large voltage V_{CC}. The input characteristics are a plot of input current I_B V_s the input voltage V_{BE} for a range of values of output voltage V_{CE}. The following important points can be observed from these characteristics curves. The characteristics resemble that of CE configuration.

1. Input resistance is high as I_B increases less rapidly with V_{BE}
2. The input resistance of the transistor is the ratio of change in base emitter voltage ΔV_{BE} to change in base current ΔI_B at constant collector emitter voltage ($V_{CE)}$ i.e... Input resistance or input impedance hie = $\Delta V_{BE} / \Delta I_B$ at V_{CE} constant.

OUTPUT CHARACTERISTICS:

A set of output characteristics or collector characteristics are a plot of out put current I_C V_S output voltage V_{CE} for a range of values of input current I_B .The following important points can be observed from these characteristics curves:-

The transistor always operates in the active region. I.e. the collector current

I_C increases with V_{CE} very slowly. For low values of the V_{CE} the I_C increases rapidly with a small increase in V_{CE} .The transistor is said to be working in saturation region.

Output resistance is the ratio of change of collector emitter voltage ΔV_{CE} , to change in collector current ΔI_C with constant I_B. Output resistance or Output impedance hoe = $\Delta V_{CE} / \Delta I_C$ at I_B constant.

Input Impedance hie = $\Delta V_{BE} / \Delta I_B$ at V_{CE} constant

Output impedance hoe = $\Delta V_{CE} / \Delta I_C$ at I_B constant

Reverse Transfer Voltage Gain hre = $\Delta V_{BE} / \Delta V_{CE}$ at I_B constant

Forward Transfer Current Gain hfe = $\Delta I_C / \Delta I_B$ at constant V_{CE}

PROCEDURE:

1. Make the connections of transistor in CE configuration circuit for plotting its input and output characteristics.
2. Take a set of readings for the variations in I_B with V_{BE} at different fixed values of output voltage V_{CE}.
3. Plot the input characteristics of CE configuration from the above readings.
4. From the graph calculate the input resistance hie and reverse transfer ratio hre by taking the slopes of the curves.
5. Take the family of readings for the variations of I_C with V_{CE} at different values of fixed I_B.
6. Plot the output characteristics from the above readings.
7. From the graphs calculate hfe ands hoe by taking the slope of the curves.

TABULAR FORMS:

INPUT CHARACTERISTICS

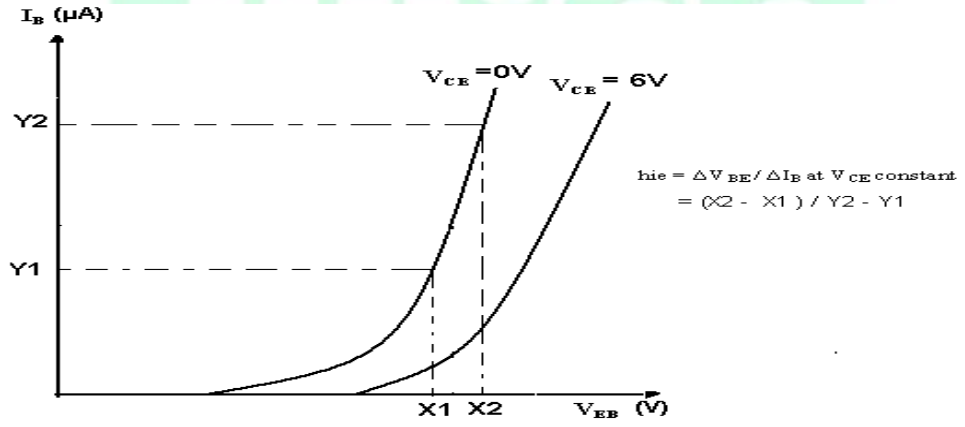
S.NO	V_{CE}=0V		V_{CE}=6V	
	V_{BE}(V)	I_B(µA)	V_{BE}(V)	I_B(µA)

OUTPUT CHARACTERISTICS

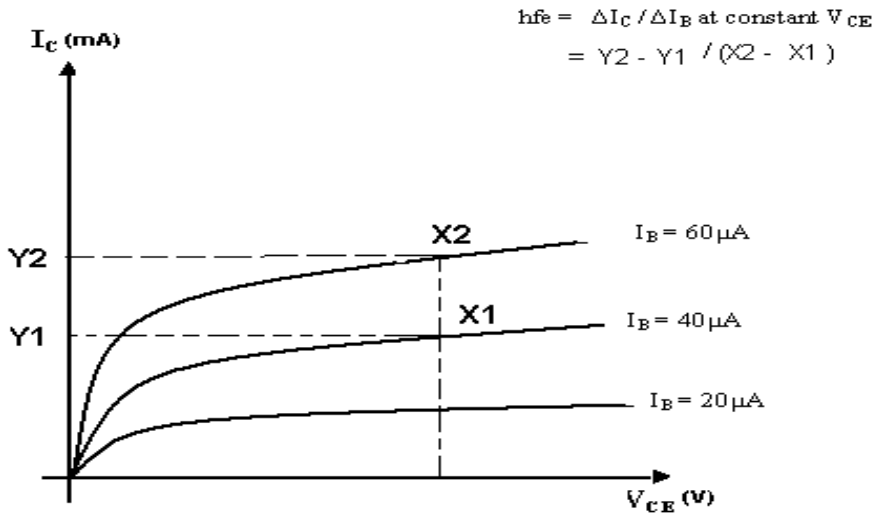
S.NO	I_B = 20 µA		I_B = 40 µA		I_B = 60 µA	
	V_{CE} (V)	I_C(mA)	V_{CE} (V)	I_C(mA)	V_{CE} (V)	I_C(mA)

MODEL WAVEFORM:

INPUT CHARACTERISTICS



OUTPUT CHARACTERISTICS



RESULT: The h-Parameters for a transistor in CE configuration are calculated from the input and output characteristics.

1. Input Impedance hie =
2. Reverse Transfer Voltage Gain hre =
3. Forward Transfer Current Gain hfe =
4. Output conductance hoe =

VIVA QUESTIONS:

1. What are the h-parameters?
2. What are the limitations of h-parameters?
3. What are its applications?
4. Draw the Equivalent circuit diagram of H parameters?
5. Define H parameter?
6. What are tabular forms of H parameters monoculture of a transistor?
7. What is the general formula for input impedance?
8. What is the general formula for Current Gain?
9. What is the general formula for Voltage gain?

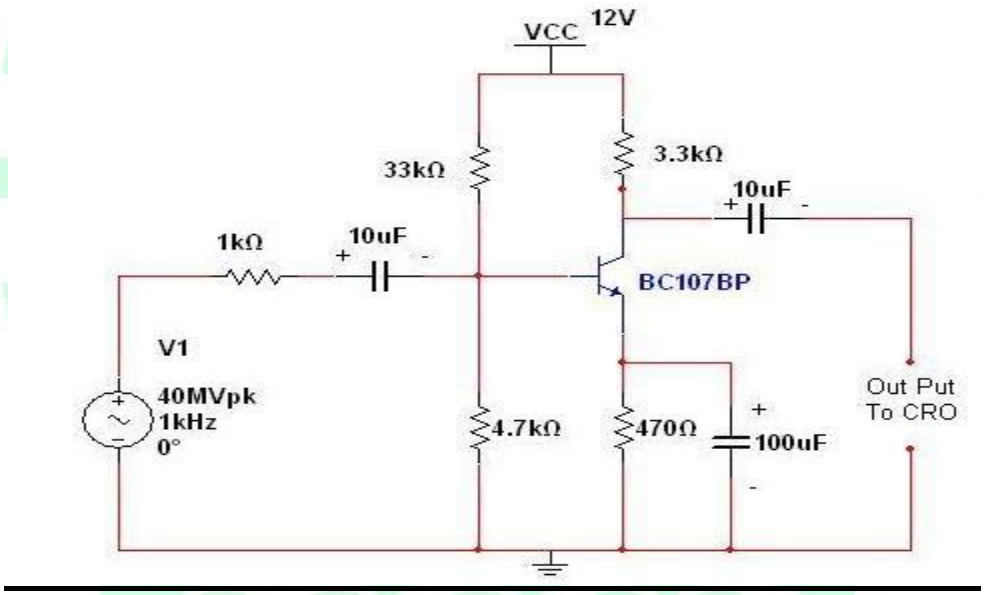
9. COMMON EMITTER AMPLIFIER

AIM: To measure the voltage gain and plot the frequency response of CE amplifier

APPARATUS:

1. Transistor BC 107-1 1 no
2. Capacitor 10µf / 25v 2 no's
3. Resistors 1K Ω, 3.3K Ω, 4.7K Ω, 470Ω, 33KΩ – each 1no.
4. Function Generator
5. Dual trace oscilloscope
6. Bread board trainer
7. D.C power supply 0-30V

CIRCUIT DIAGRAM:



THEORY:

The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current. When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

PROCEDURE:

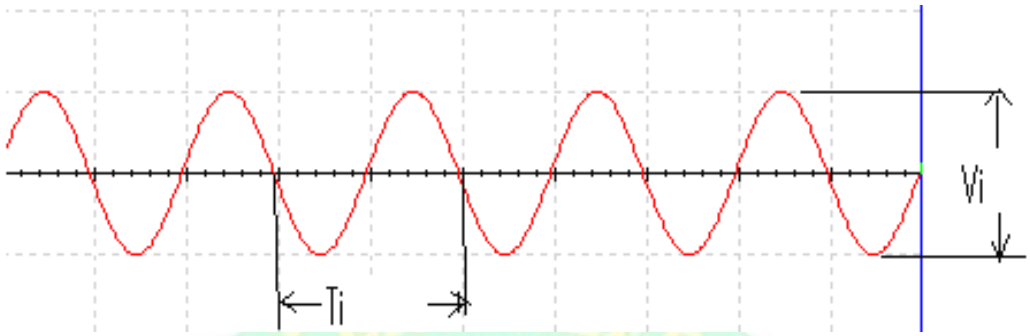
1. Make the connections as per the circuit diagram.
2. Make the Connection of signal generator output to input terminals of the circuit and channel –1 of dual trace CRO
3. Make the Connection of output terminal of the circuit to channel – 2 of the dual trace CRO
4. Set the signal generator output at 10mv constant to the circuit
5. Set the signal generator output at 10mvconstant, sine wave at 100 Hz
6. Vary the signal generator frequency from 100 Hz to 500 kHz as per the table given and note the corresponding output voltage
7. Calculate the gain Av=Vo/Vi

TABULAR FORM:

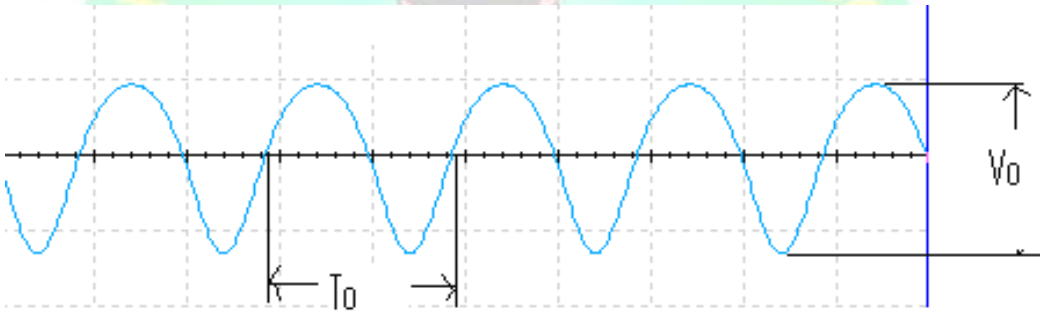
Input Voltage= 40 mV

S.NO	INPUT FREQUENCY (HZ)	OUTPUT VOLTAGE (Vo)	GAIN Av=Vo/Vi	GAIN in db 20 log (Av)
1	100			
2	200			
3	300			
4	400			
5	500			
6	600			
7	700			
8	800			
9	900			
10	1K			
11	2K			
12	3K			
13	4K			
14	5K			
15	6K			
16	7K			
17	8K			
18	9K			
19	10K			
20	20K			
21	30K			
22	40K			
23	50K			
24	100K			
25	200K			
26	300K			
27	400K			
28	500K			

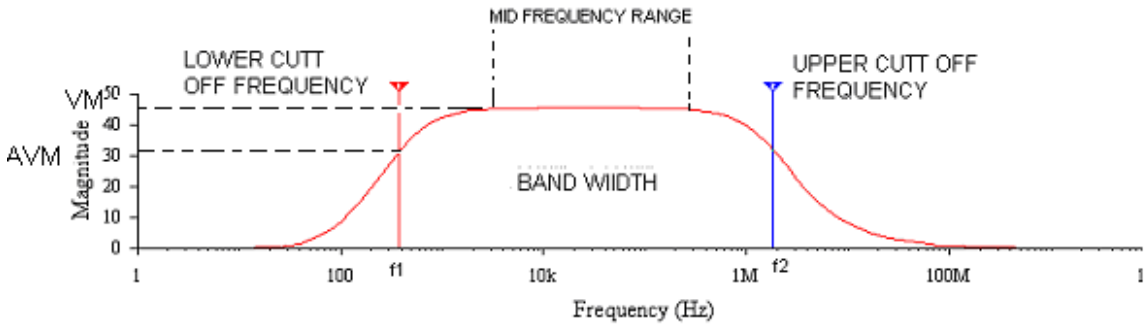
INPUT WAVE FORM:



OUTPUT WAVE FORM



FREQUENCY RESPONSE



GRAPH:

Plot the graph frequency verses gain (db) on a semi log sheet

RESULT:

Verified the voltage gain and frequency response of CE amplifier.

QUESTIONS:

1. What is phase difference between input and output waveforms of CE amplifier?
2. What type of biasing is used in the given circuit?
3. If the given transistor is replaced by a p-n-p, can we get output or not?
4. What is effect of emitter-bypass capacitor on frequency response?
5. What is the effect of coupling capacitor?
6. What is region of the transistor so that it is operated as an amplifier?
7. How does transistor acts as an amplifier?
8. Draw the h-parameter model of CE amplifier?
9. What type of transistor configuration is used in intermediate stages of a multistage amplifier?
10. What is Early effect?

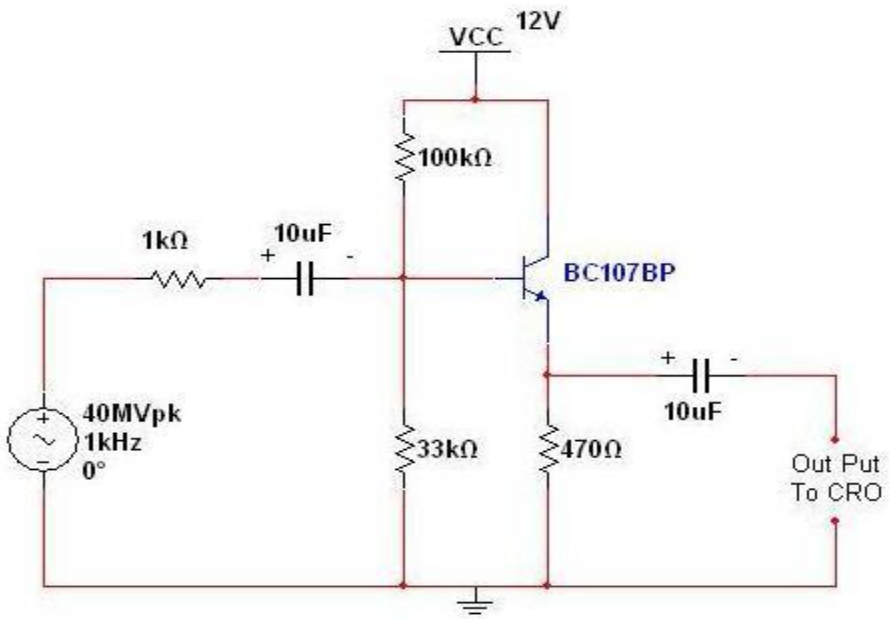
10. COMMON COLLECTOR AMPLIFIER (EMITTER FOLLOWER)

AIM: To measure the voltage gain and plot the frequency response of CC amplifier

APPARATUS:

1. Transistor BC 107- 1 no
2. Capacitor 10µf / 25v - 2 no's
3. Resistors 1K Ω, 33K Ω, 470Ω, 100 KΩ - 1 each
4. Function Generator
5. Dual trace oscilloscope
6. Bread board trainer
7. D.C power supply 0-30V

CIRCUIT DIAGRAM:



THEORY:

In common-collector amplifier the input is given at the base and the output is taken at the emitter. In this amplifier, there is no phase inversion between input and output. The input impedance of the CC amplifier is very high and output impedance is low. The voltage gain is less than unity. Here the collector is at ac ground and the capacitors used must have a negligible reactance at the frequency of operation.

This amplifier is used for impedance matching and as a buffer amplifier. This circuit is also known as emitter follower.

PROCEDURE:

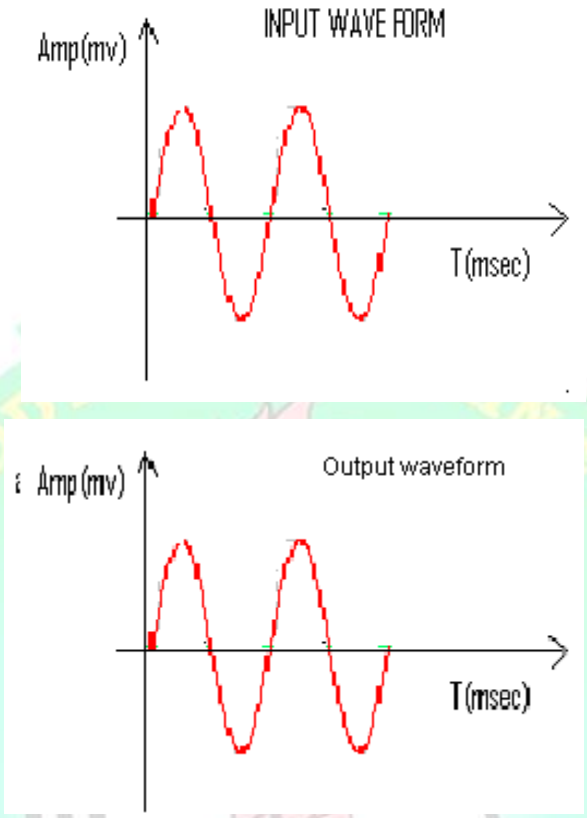
1. Make the connections as per the circuit diagram
2. Make the Connection of signal generator output to input terminals of the circuit and channel – 1 of dual trace CRO
3. Make the Connection of output terminal of the circuit to channel – 2 of the dual trace CRO
4. Set the power supply voltage to 9V and connect to the circuit
5. Set the signal generator output at 100mv constant, sine wave at 100 Hz frequency
6. Vary the signal generator frequency from 100 Hz to 500 kHz as per the table given and note the corresponding output voltage
7. Calculate the gain Av=Vo/Vi

TABULAR FORM:

Input Voltage=2 V

S.NO	INPUT FREQUENCY (HZ)	OUTPUT VOLTAGE	GAIN Av=Vo/Vi	GAIN in db 20 log (Av)
1	100			
2	200			
3	300			
4	400			
5	500			
6	600			
7	700			
8	800			
9	900			
10	1K			
11	2K			
12	3K			
13	4K			
14	5K			
15	6K			
16	7K			
17	8K			
18	9K			
19	10K			
20	20K			
22	50K			
23	100K			

WAVEFORMS:



GRAPH: Plot the graph frequency verses gain (db) on a (semi log) sheet

RESULT: Verified the voltage gain and frequency response of CC amplifier

QUESTIONS:

1. What are the applications of CC amplifier?
2. What is the voltage gain of CC amplifier?
3. What are the values of input and output impedances of the CC amplifier?
4. To which ground the collector terminal is connected in the circuit?
5. Identify the type of biasing used in the circuit?
6. Give the relation between α, β and γ.
7. Write the other name of CC amplifier?
8. What are the differences between CE, CB and CC?
9. When compared to CE, CC is not used for amplification. Justify your answer?
10. What is the phase relationship between input and output in CC?

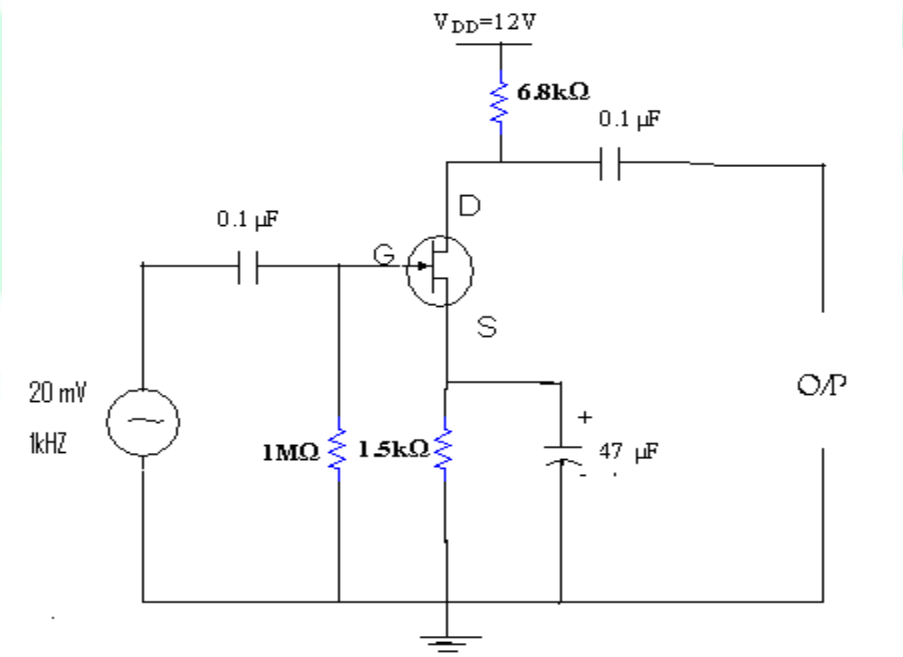
11. FET AMPLIFIER (COMMON SOURCE)

AIM : To obtain the frequency response of single stage common source JFET amplifier

APPARATUS:

1. FET BFW 11 1.no.
2. Capacitors 0.1µf 2 no's
3. Capacitors 47µf 1 no's
4. Resisters 1MΩ, 1.5KΩ, 6.8KΩ each 1 No.
5. Function Generator
6. CRO
7. Bread Board
8. 0 – 30v, 1A Dual Channel Power Supply

CIRCUIT DIAGRAM:



THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak- signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain.

The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors

exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide-semiconductor FET (MOSFET).

The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle.

The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes.

PROCEDURE:

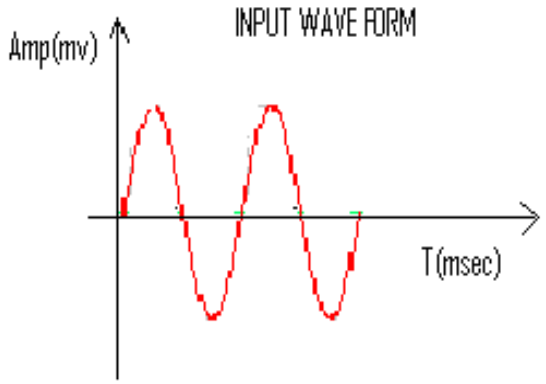
1. Make the connections as per the circuit diagram
2. Make the Connection of signal generator output to input terminal of the circuit and channel –1 of dual trace CRO
3. Make the Connection of output terminal of the circuit to channel – 2 of the dual trace CRO
4. Set the D.C power supply voltage to 9v and connect to the circuit
5. Set the signal generator output at 50mv constant of sine wave
6. Vary the signal generator frequency from 50 Hz to 1 MHz as per the table given and note the corresponding output voltage
7. Calculate the gain in db 20 log Vo/Vi.

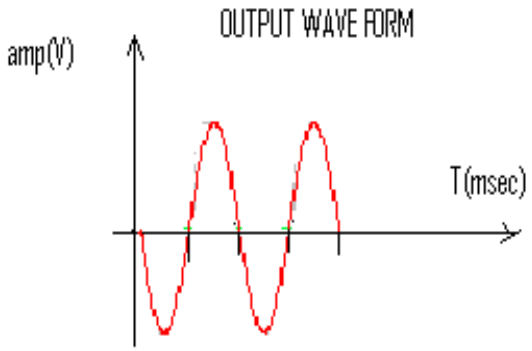
TABULAR FORM:

S.NO	Frequency of I/P Signal (Hz)	O/P Voltage(V)	Gain Av=Vo/Vi	Gain in db 20 log Av
1	50			
2	100			
3	200			
4	500			
5	1K			
6	5K			
7	10K			
8	20K			
9	30K			
10	40K			
11	50K			
12	60K			
13	70K			
14	80K			
15	90K			
16	100K			
17	200K			
18	300K			
19	400K			
20	500K			
21	1M			

GRAPH: Plot the graph frequency verses gain (db) on a semi log sheet

MODEL GRAPH:





RESULT: Verified the voltage gain and frequency response of single stage common source JFET Amplifier

VIVA QUESTIONS

1. What is the difference between FET and BJT?
2. FET is unipolar or bipolar?
3. Draw the symbol of FET?
4. What are the applications of FET?
5. FET is voltage controlled or current controlled?
6. Draw the equivalent circuit of common source FET amplifier?
7. What is the voltage gain of the FET amplifier?
8. What is the input impedance of FET amplifier?
9. What is the output impedance of FET amplifier?
10. What are the FET parameters?
11. What are the FET applications?

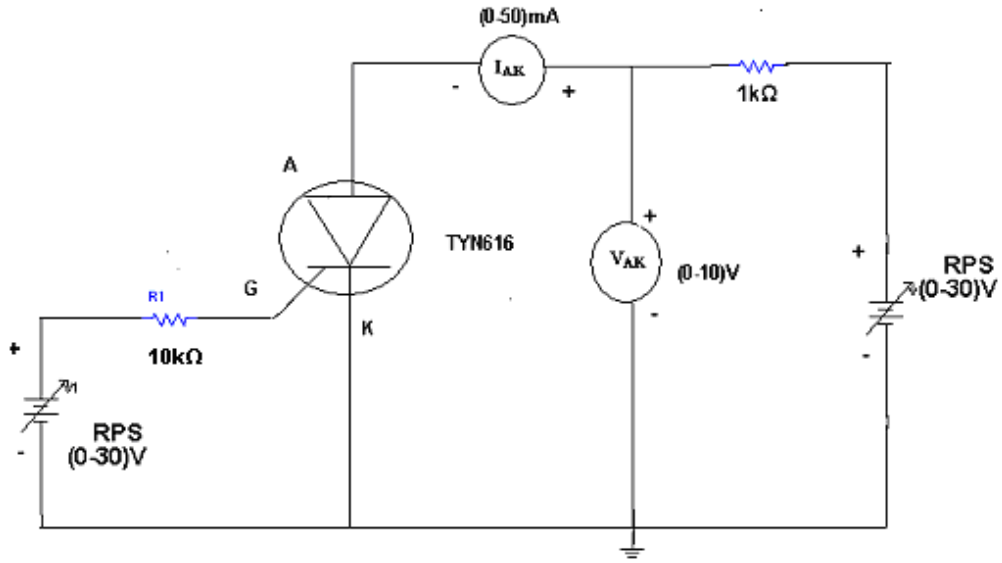
12. SCR CHARACTERISTICS

AIM: To find the latching current and holding current of a given SCR and plot the V- I characteristics of the Silicon Controlled Rectifier.

APPARATUS REQUIRED:

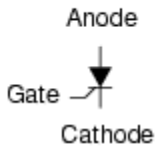
1.	SCR TYN 410	1No.
2.	Resistor 1K, (½ Watt)	1No.
	10K	1No.
3.	Ammeter 0 – 20 mA (Analog type).	1No.
	0 – 100 mA (Analog type).	1No.
4.	Volt meter 0 – 30 V (Analog type).	1No.
5.	0 – 30V Dual Channel Power Supply	1No.
6.	Connecting Wires	
7.	Bread Board	1No.

CIRCUIT DIAGRAM:



THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J_1, J_2, J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K, and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive
with respect to cathode.



Schematic symbol

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cut off. When anode voltage is increased J_2 tends to breakdown.

When the gate positive, with respect to cathode J_3 junction is forward biased and J_2 is reverse biased .Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing, anode current increase is in extremely small current junction J_2 break down and SCR conducts heavily.

When gate is open thee break over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

PROCEDURE:

1. Make the connections as per the circuit diagram.
2. Set gate current I_G equal to firing current in CH -1, vary anode to cathode voltage in CH -2 and carefully observe the voltmeter reading.
3. Check the point where SCR voltage (V_{AK}) suddenly drops and sudden increase anode current
4. Note down the current at that point is called latching current.
5. Increase the anode to cathode supply till it is maximum i.e 30V in Ch – 2 power supply and note the maximum value of current read in the Ammeter.
6. Now open the gate terminal and decrease the anode to cathode voltage V_{AK} (Ch-2) power supply.
7. By decreasing V_{AK} slowly at one point the deflection of the ammeter suddenly reduces to Zero. Note down that point and that point is called holding current.
8. Plot the graph between V_{AK} and I_A and I_G.

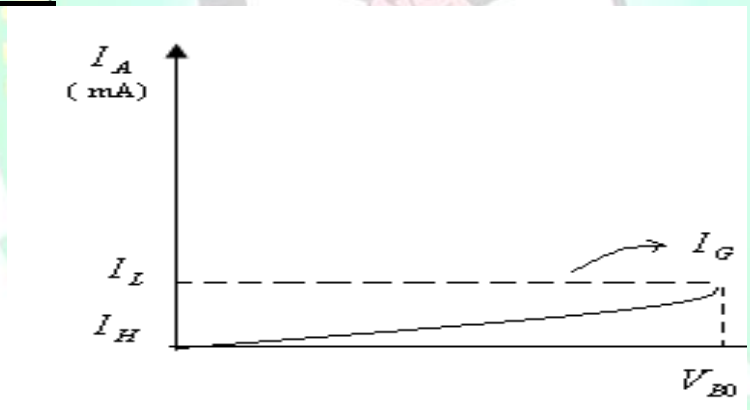
TABULAR FORM :

Firing Current

I_G =

Sl. No	V_{AK} **(Volts)**	I_A **(mA)**
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

MODEL GRAPH :



RESULT:

V-I characteristics of SCR is plotted and Values are obtained as

Parameter	Practical
Break over voltage(V_{B0})	
Latching Current (I_L)	
Holding Current (I_H)	
Maximum Current	

VIVA QUESTIONS

1. What the symbol of SCR?
2. IN which state SCR turns of conducting state to blocking state?
3. What are the applications of SCR?
4. What is holding current?
5. What are the important type's thyristors?
6. How many numbers of junctions are involved in SCR?
7. What is the function of gate in SCR?
8. When gate is open, what happens when anode voltage is increased?
9. What is the value of forward resistance offered by SCR?
10. What is the condition for making from conducting state to non conducting state?

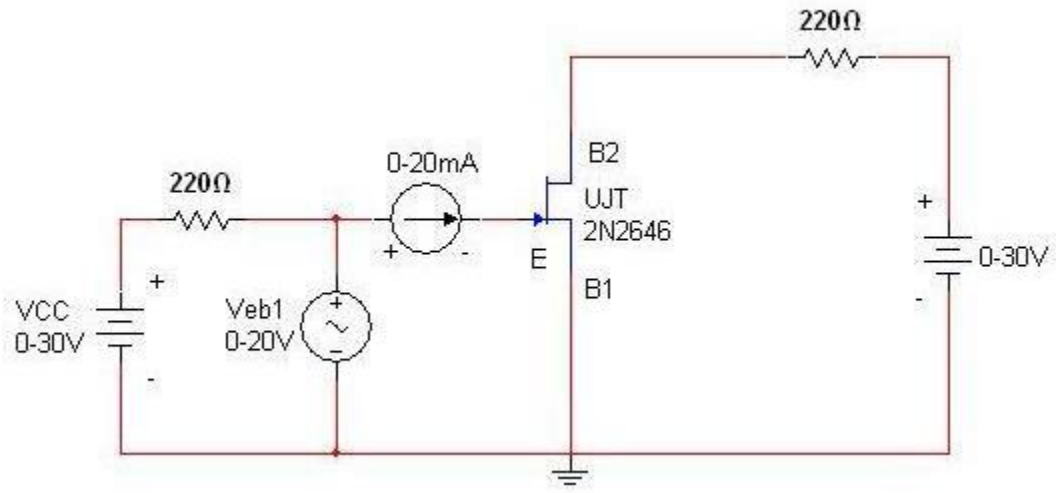
13. UJT CHARACTERISTICS

AIM: To observe the characteristics of UJT and to calculate the Intrinsic Stand-Off Ratio (η).

APPARATUS:

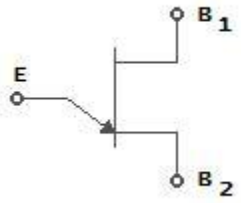
1. Regulated Power Supply (0-30V, 1A) - 2Nos
2. UJT 2N2646
3. Resistors 220Ω – 2Nos
4. Multimeters - 2Nos
5. Breadboard
6. Connecting Wires

CIRCUIT DIAGRAM:



THEORY:

A Uni junction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Uni junction Transistor (UJT) has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is Open-circuit is called inter base resistance. The original uni junction transistor, or UJT, is simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.



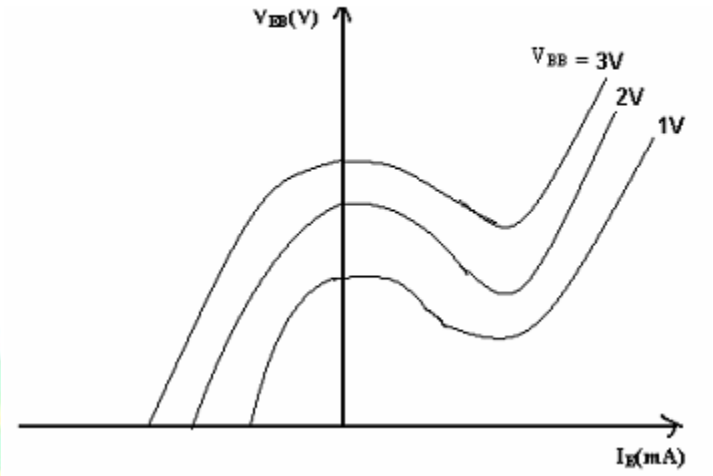
Circuit symbol

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits. When the emitter voltage reaches V_p, the current starts to increase and the emitter voltage starts to decrease. This is represented by negative slope of the characteristics which is referred to as the negative resistance region, beyond the valley point ,R_{B1} reaches minimum value and this region, V_{EB} proportional to I_E.

PROCEDURE:

1. Make the connections as per the circuit diagram.
2. Output voltage is fixed at a constant level and by varying input voltage corresponding emitter current values are noted down.
3. Repeat the procedure for different values of output voltages.
4. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using $\eta = (V_p - V_D) / V_{BB}$
5. A graph is plotted between V_{EE} and I_E for different values of V_{BE}.

MODEL GRAPH:



OBSEVATIONS:

V_{BB}=1V		V_{BB}=2V		V_{BB}=3V	
V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)	V_{EB}(V)	I_E(mA)

CALCULATIONS:

$$V_P = \eta V_{BB} + V_D$$

$$\eta = (V_P - V_D) / V_{BB}$$

$$\eta = (\eta_1 + \eta_2 + \eta_3) / 3$$

RESULT:

The characteristics of UJT are observed and the values of Intrinsic Stand-Off ratio is calculated.

VIVA QUESTIONS

1. What is the symbol of UJT?
2. Draw the equivalent circuit of UJT?
3. What are the applications of UJT?
4. Formula for the intrinsic stand off ratio?
5. What does it indicates the direction of arrow in the UJT?
6. What is the difference between FET and UJT?
7. Is UJT is used an oscillator? Why?
8. What is the Resistance between B_1 and B_2 is called as_____
9. What is its value of resistance between B_1 and B_2
10. Draw the characteristics of UJT?

11.TWO STAGE RC COUPULED AMPLIFIER

AIM:

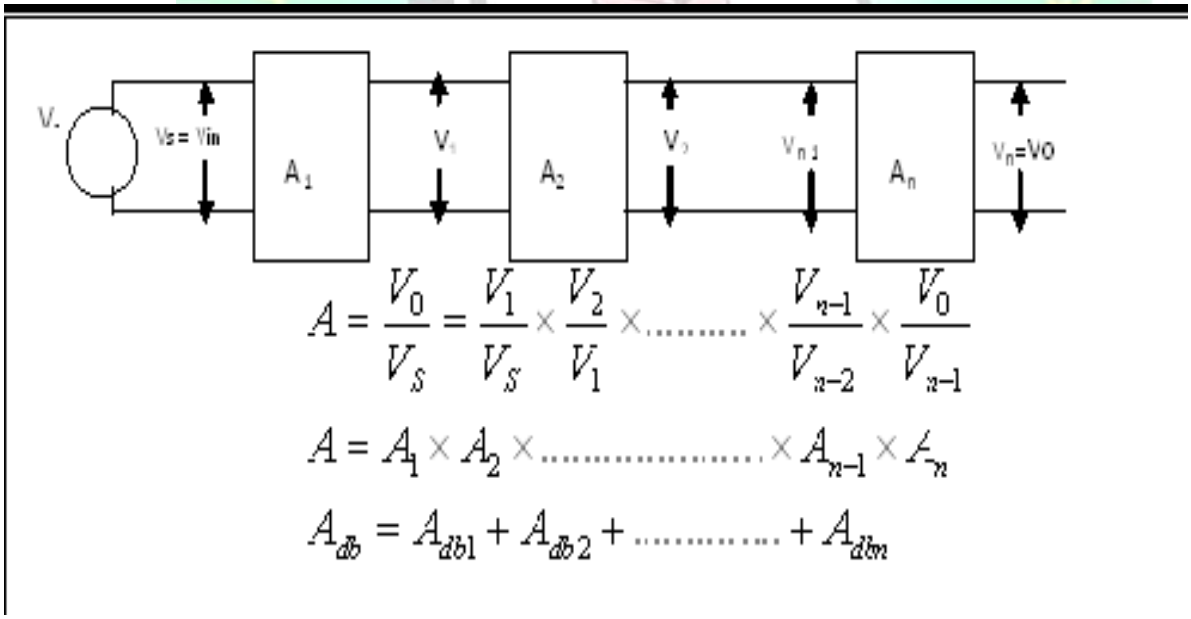
To cascade two identical stages of a CE amplifier using RC coupling and compare Band Width, Mid Band Gain of Individual and Overall Stages.

APPARATUS:

1. Function Generator
2. DC Power Supply
3. Cathode Ray Oscilloscope
4. Transistor : BC 107 – 2no's
5. Resistors : 1kΩ - 3nos, 2.2kΩ - 2no's, 10kΩ - 2no's, 47kΩ - 2no's , 100kΩ - 2no's
6. Capacitors - 10μF – 3no's, 100μF – 2no's

THEORY:

Voltage level of a signal can be raised to the desired level if we use more than one stage. When a no of amplifier stages are used in succession, it is called a multistage amplifier or cascade amplifier. Much higher gain can be obtained from multistage amplifier.



$$A = \frac{V_0}{V_S} = \frac{V_1}{V_S} \times \frac{V_2}{V_1} \times \ldots\ldots\ldots \times \frac{V_{n-1}}{V_{n-2}} \times \frac{V_0}{V_{n-1}}$$

$$A = A_1 \times A_2 \times \ldots\ldots\ldots\ldots\ldots \times A_{n-1} \times A_n$$

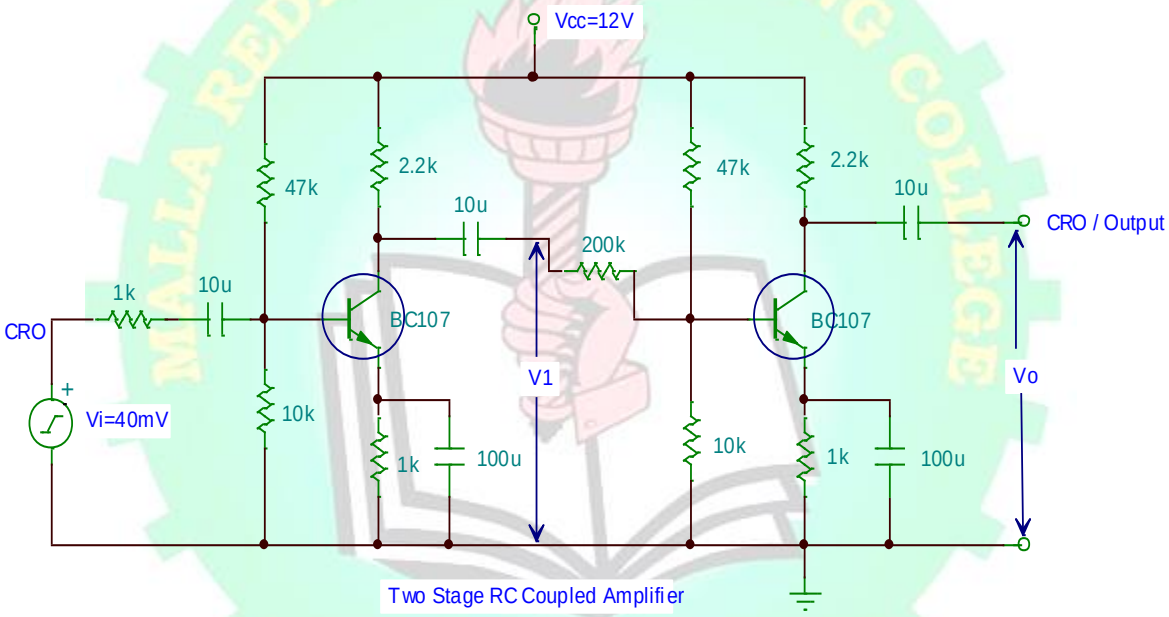
$$A_{db} = A_{db1} + A_{db2} + \ldots\ldots\ldots\ldots + A_{dbn}$$

In a multistage amplifier, the output of one stage makes input of next stage. A suitable coupling network between 2 stages must be used so that a minimum loss of voltage occurs when the signal passes through this network, to the next stage. Also the dc voltage at the output of one stage should not be permitted to go to input of next. If it does, the biasing conditions of next stage are disturbed. The 3 generally used coupling schemes are

1) Resistor – Capacitor Coupling
2) Transformer Coupling
3) Direct Coupling

RC coupling is most widely used scheme. In this method, signal developed across the collector resistor Rc of first stage is coupled to the base of the second stage through a capacitor. This capacitor blocks the dc voltage of first stage from reaching the base of second stage. In this way the dc biasing of next stage is not interfered with.

CIRCUIT DIAGRAM:



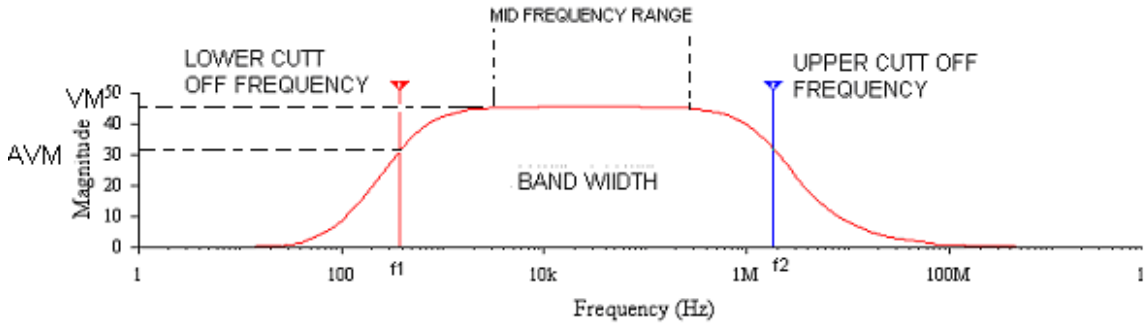
PROCEDURE:

1. Make the connections as per the circuit diagram.
2. Check the outputs of First stage and Second Stage individually.
3. Now couple the two stages using 10μF capacitor.
4. Observe the overall output. It will be clipped at both positive & negative peaks.
5. Place a 100kΩ resistor to attenuate the output of first stage before it reaches second stage.
6. Vary the frequency of input and note down the output voltages of individual stages and overall stages.
7. Calculate gain, gain in dB of individual and overall stages, theoretically and practically.
8. Plot Frequency response curves for individual and overall stages.

TABULAR COLUMN:

		FIRST STAGE			SECOND STAGE		
S.NO	INPUT FREQUENCY (HZ)	OUTPUT VOLTAGE (Vo)	GAIN Av=Vo/Vi	GAIN in db 20 log (Av)	OUTPUT VOLTAGE (Vo)	GAIN Av= Vo/Vi	GAIN in db 20 log (Av)
1	100						
2	200						
3	300						
4	400						
5	500						
6	600						
7	700						
8	800						
9	900						
10	1K						
11	2K						
12	3K						
13	4K						
14	5K						
15	6K						
16	7K						
17	8K						
18	9K						
19	10K						
20	20K						
22	50K						
23	100K						

EXPECTED GRAPH:



RESULT:

	Band Width	mid Band Gain
Single stage	_____	_____
Overall	_____	_____

VIVA QUESTIONS:

1. How many coupling scheme are there? Name it.
2. Which is the best coupling scheme?
3. What is mean by coupled?
4. What is an amplifier?